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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,410	06/24/2005	Carl Glasse	1217/204	4245

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EXAMINER	
LE, DUNG ANH	
ART UNIT	PAPER NUMBER
2818	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,410	GLASSE ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,9,10 and 14-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-4,9-10,14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections

Set of claims 1-4, 9-11

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 4 and 11 are rejected under 35 USC 102 (b) as being anticipated by Yoshikawa (4925807).

Yoshikawa teaches thin film transistor on a substrate comprising: a semiconductor layer having a first doped region 27b and a second doped region 27a in between a first further doped region 28b and a second further doped region 28a , and having an undoped region in between the first doped region and the second doped region (particularly figs. 2b, 4b and 5b and related texts) , the first doped region and the second doped region having a lower conductivity than the first further doped region and the second further doped region; and an oxide layer 22 partially covering a surface of the semiconductor layer, the oxide layer carrying:

a conductive gate 23 over the undoped region having a first side and a second side substantially perpendicular to the oxide layer; a first spacer 24 and a second spacer adjacent to the first side and second side of the conductive gate respectively; a first insulating spacer 29 adjacent to a side of the first spacer opposite the first side of the conductive gate; and a second insulating spacer adjacent to a side of the second spacer opposite the second side of the conductive gate; the thin film transistor further comprising: a first conductive contact 30/30b with the first further doped region 28a ; and a second conductive contact with the second further doped region 28b.

Regarding claim 2, wherein the first spacer 25 and the second spacer comprise a conductive material (col. 3, line(s) 15-20) .

Regarding claim 3,wherein the first conductive contact and the second conductive contact comprise a silicide layer 30b (col 5,lines 25-30).

Regarding claim 4, wherein the semiconductor layer 21 comprises a polycrystalline silicon material.

Regarding claims 11, thin film transistor substantially as described herein with reference to the drawings (particularly figs. 2b, 4b and 5b and related texts) .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9- 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Yoshikawa in view of the following remark.

Yoshikawa teaches the claimed invention as applied to claim 1 except for an electronic device comprising an active matrix array coupled to a first driver circuit arrangement and a second driver circuit arrangement, the first driver circuit arrangement and the second driver circuit arrangement being coupled to a power supply, at least one of the matrix array, the first driver circuit arrangement and the second driver circuit arrangement comprising a plurality of claimed thin film transistors and wherein the power supply comprises battery means as cited in current claims 9-10.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form an electronic device comprising an active matrix array coupled to a first driver circuit arrangement and a second driver circuit arrangement, the

first driver circuit arrangement and the second driver circuit arrangement being coupled to a power supply, at least one of the matrix array, the first driver circuit arrangement and the second driver circuit arrangement comprising a plurality of claimed thin film transistors and wherein the power supply comprises battery means, the above mentioned limitation is commonly used to greatly enhance the efficientcy of the claimed thin film transistor and its superior electronic characteristic can be achieved, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the particular practice.

Response to Amendment

Claims 2, 5-8, and 11-13 have been canceled. Claims 1 and 9 have been amended. New Claims 14-26 have been added. Claims l, 3, 4, 9, 10, and 14-26 remain pending in this application.

Applicant's argument filed 1/16/2007 have been fully considered but they are not deemed to be persuasive. Applicant argues that:

"Claims 1-4 and 11 are rejected under 35 USC 102(b) as being anticipated by Yoshikawa (U.S. Patent No. 4,925,807). This rejection is respectfully traversed.

Applicant submits that at least the subject matter of previously presented claim 2 should be patentable over Yoshikawa. Claim 2 recites that the first and second spacers are conductive. The first and second conductive spacers are respectively between the

gate and the respective first and second insulating spacers. Claim 2 has been canceled, and claim 1 has been amended to incorporate the limitations of claim 2. Specifically, claim 1 as amended now recites a conductive gate; a first conductive spacer and a second conductive spacer adjacent to the first side and second side of the conductive gate respectively; a first insulating spacer adjacent to a, side of the first conductive spacer opposite the first side of the conductive gate; and a second insulating spacer adjacent to a side of the second conductive spacer opposite the second side of the conductive gate. Yoshikawa does not disclose a conductive spacer between the gate and a insulating spacer. In contrast, Yoshikawa discloses the reverse, i.e., an. insulating structure 24 between the gate 23 and the conductive structure 25.

Claim 1 is therefore not anticipated by and is patentable over Yoshikawa. It follows that all the claims dependent from claim 1 are likewise not anticipated and are patentable over Yoshikawa. The dependent claims further recited Limitations that further distinguish from Yoshikawa.

In the event the Examiner maintains the rejection of claim 1 on a new ground of rejection in the next action, such action should not be made final, since such new ground would not be necessitated by the present amendment to claim 1, which only included the subject matter of previously presented (now canceled) claim 1.

Claim Rejections Under 35 USC 103. Claims 9 and 10 are rejected under 35 USC 103(a) as being unpatentable over Yoshikawa. Given the traversal of base claim 1, the rejection of claims 9 and 10 are moot. Claims 9 mad 10 are patentable over Yoshikawa

for at least the same reasons for base claim 1.

New claims 14 - 26 have been added to round out the coverage of the present invention. Applicant respectfully submits that these new claims are patentable over Yoshikawa for at least the same reasons presented above."

Contrary to applicant's argument, especially see figs. 5A-5B and refer to related text of Yoshikawa.

Regarding claim 1, Yoshikawa teaches a first conductive spacer 25 (col 3, line 15) and a second conductive spacer 15 adjacent to the first side and second side of the conductive gate 23 (col 3, line 45) respectively; a first insulating spacer 29 adjacent to a side of the first conductive spacer 25 opposite the first side of the conductive gate 23; and a second insulating spacer 229 adjacent to a side of the second conductive spacer opposite the second side of the conductive gate. Yoshikawa does disclose a conductive spacer between the gate and a insulating spacer.

Regarding claim 14 (newly added claim), a plurality of metric elements, each comprising a thin film transistor (col 2, lines 50-55).

Set of claims 15-26

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15-26 are rejected under 35 USC 102 (b) as being anticipated by Sanchez (5,091,763).

Sanchez teaches a thin film transistor (especially see figs. 1, 3-4 and refer to related text) , comprising:

a substrate 12;

a semiconductor layer supported on the substrate (especially see fig. 1 and refer to related text) , including an undoped region, a first doped region 18a and a second doped region 18b, and a first further doped region 22a, and a second further doped region 22b, wherein the first doped region is between the doped region and the first further doped region, and the second doped region is between the undoped region and the first further doped region;

a gate 16 supported above the semiconductor layer;

a first insulating spacer 28a disposed at a first side of the gate 16 and a second insulating spacer 28b disposed at a second side of the gate; and

a first conductive spacer 20a between the first insulating spacer 28a and the gate 16, and a second conductive spacer 20b between the second insulating spacer 28b and the gate 16.

Regarding claim 16, wherein, the first conductive spacer 20a is directly above the first doped region 18b and the second conductive spacer is directly above the second

doped region.

Regarding claim 17, wherein the first side of the gate 16 is aligned with a first edge of the undoped region 18a, and the second side of the gate is aligned with a second edge of the undoped region 18b.

Regarding claim 1 8, wherein a first edge of the first conductive spacer 20a away from the gate is aligned with a first edge of the first doped region away from the undoped region, and a second edge of the second conductive spacer 20b away from the gate is aligned with a second edge of the second doped region away from the undoped region (especially see fig. 3 and refer to related text).

Regarding claim 19, further comprising: an oxide layer coveting the undoped region, the first doped region and the second doped region, and partially coveting the first further doped region and the second further doped region, wherein the oxide layer supports the gate, the first conductive spacer, the second conductive spacer, the first insulating spacer, and the second insulating spacer.

Regarding claim 20, wherein a first edge of the first insulating spacer 28a away form the first conductive spacer 20a is aligned with a first edge of the oxide layer, and a second edge of the second insulating spacer 28b away from the second conductive spacer 20b is aligned with a second edge of the oxide layer.

Regarding claim 21, further comprising: a first conductive contact 26 with the first further doped region; and a second conductive contact 26 with the second further doped region (especially see fig. 4 and refer to related text).

Regarding claim 22, wherein the conductive spacer 20a is adjoining a first side of the gate 16 , and the second conductive spacer 20b is adjoining a second side of the gate 16.

Regarding claim 23, wherein the first insulating spacer 28a is adjoining the first conductive spacer 20a away from the gate, and the second insulating spacer is adjoining the second, conductive spacer away from the gate.

Regarding claim 25, an active matrix array as in claim 24; and at least one driver circuit operatively coupled to the active matrix array (especially see fig. 4 and refer to related text) .

Regarding claim 26, method for producing a thin film transistor as in claim 15 (col 3, line 15).

Set of claims 15-26, Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, M. Smith can be reached on (571) 272-1907. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818